IN THE CLAIMS:

Claims 1-3, 6, 8-13, 15 and 19-22 have been amended herein. Claim 23 has been added as a new claim. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently amended) A printed circuit board, comprising:

a substrate having at least one electrically insulative layer; and

a plurality of conductive trace layers formed on opposing sides of the at least one electrically insulative layer, wherein at least one of the plurality of conductive trace layers includes a plurality of conductive traces including at least two signal traces and at least one voltage reference trace, the plurality of conductive traces being configured such that the at least one voltage reference trace is between the at least two signal traces, the at least one voltage reference trace also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace.

2. (Currently amended) The printed circuit board of claim 1, wherein at least one of the plurality of conductive traces includes at least one direction change in the length thereof over the at least one electrically insulative layer.

3. (Currently amended) The printed circuit board of claim 1, wherein the at least one electrically insulative layer comprises a plurality of insulative layers, each insulative layer separated by at least one conductive trace layer.

4. (Original) The printed circuit board of claim 1, wherein at least one of the conductive trace layers is a voltage reference plane.

5. (Original) The printed circuit board of claim 4, wherein the at least one voltage reference trace is coupled to the voltage reference plane.

6. (Currently amended) The printed circuit board of claim 1, further comprising a passivation layer deposited on at least one of the plurality of conductive trace layers.

7. (Previously presented) The printed circuit board of claim 1, wherein the at least one electrically insulative layer comprises two electrically insulative layers separated by a conductive layer, and wherein the at least one voltage reference trace is electrically coupled to the conductive layer.

8. (Currently amended) The printed circuit board of claim 1, wherein the at least one voltage reference trace is electrically coupled to at least one voltage reference bus.

9. (Currently amended) The printed circuit board of claim 1, wherein at least a portion of the plurality of conductive traces are embodied as vias.

10. (Currently amended) A printed circuit board, comprising at least one electrically insulative layer and at least one electrically conductive layer, the at least one electrically conductive layer comprising a voltage reference portion and at least one signal trace electrically isolated from the voltage reference portion, wherein the voltage reference portion has a greater surface area than the at least one signal trace, and wherein the voltage reference portion comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace.

11. (Currently amended) The printed circuit board of claim 10, wherein a majority of the at least one electrically conductive layer is comprised of the voltage reference portion.

12. (Currently amended) The printed circuit board of claim 10, wherein the voltage reference portion comprises a voltage reference bus with at least one voltage reference trace extending from the voltage reference bus.

13. (Currently amended) An electronic device, comprising:

at least one electrically insulative layer; and

at least one conductive layer, the at least one conductive layer comprising a voltage reference bus having at least one voltage reference trace extending therefrom and at least two signal traces electrically isolated from the at least one voltage reference trace, wherein the at least one voltage reference trace and the at least two signal traces are configured such that each signal trace is separated from each other signal trace by the at least one voltage reference trace, and wherein the at least one voltage reference trace is spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace.

14. (Previously presented) The electronic device of claim 13, further comprising a passivation layer deposited on the at least one conductive layer.

15. (Currently amended) A printed circuit board, comprising:

at least one voltage reference plane substantially coextensive with a portion of a substrate; and

at least one signal trace substantially coplanar with the at least one voltage reference plane and electrically isolated therefrom, the at least one voltage reference plane having a substantially greater surface area than the at least one signal trace, and wherein the

voltage reference plane comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace.

16. (Original) The printed circuit board of claim 15, wherein the at least one signal trace is electrically isolated from the at least one voltage reference plane by at least one trough.

17. (Previously presented) The printed circuit board of claim 15, further comprising a passivation layer deposited on the at least one signal trace and the at least one voltage reference plane.

18. (Original) The printed circuit board of claim 15, wherein the at least one voltage reference plane is a substantially continuous voltage reference plane.

19. (Currently amended) A printed circuit board, comprising at least one voltage reference plane having at least one coplanar signal trace isolated therefrom, wherein the at least one voltage reference plane includes a surface area greater than any one signal trace, and wherein the voltage reference plane comprises a voltage reference bus having at least one voltage reference trace extending therefrom.

20. (Currently amended) An electronic system, comprising:

a processor;

a memory device;

at least one input device;

at least one output device; and

at least one data storage device;

wherein at least one of the processor, the memory device, the at least one input device, the at least one output device and the at least one data storage device includes a printed circuit board comprising:

a substrate having at least one electrically insulative layer; and

a plurality of conductive trace layers formed on opposing sides of the at least one electrically insulative layer, wherein each of the plurality of conductive trace layers includes a plurality of conductive traces including at least two signal traces and at least one voltage reference trace, the plurality of conductive traces being configured such that the at least one voltage reference trace is between the at least two signal traces, the at least one voltage reference trace also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace.

21. (Currently amended) The electronic system of claim 20, wherein at least one of the at least two signal traces includes at least one non-linear path over the at least one electrically insulative layer.

22. (Currently amended) An electronic system, comprising:

a processor;

a memory device;

at least one input device;

at least one output device; and

at least one data storage device;

wherein at least one of the processor, the memory device, the at least one input device, the at least one output device and the at least one data storage device includes a printed circuit board comprising:

at least one voltage reference plane substantially coextensive with a portion of a substrate; and

at least one signal trace substantially coplanar with the at least one voltage reference plane and electrically isolated therefrom, the at least one voltage reference plane having a substantially greater surface area than the at least one signal trace, and wherein the voltage reference plane comprises at least one voltage reference trace spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace..

23. (New) An electronic system, comprising:

a processor;

a memory device;

at least one input device;

at least one output device;

at least one data storage device; and

a printed circuit board comprising:

a substrate having at least one electrically insulative layer; and

a plurality of conductive trace layers formed on opposing sides of the at least one electrically insulative layer, wherein each of the plurality of conductive trace layers includes a plurality of conductive traces including at least two signal traces and at least one voltage reference trace, the plurality of conductive traces being configured such that the at least one voltage reference trace is between the at least two signal traces, the at least one voltage reference trace also spatially periodically coupled to a reference voltage at intervals predetermined to maintain a substantially consistent reference voltage throughout the at least one voltage reference trace.

IN THE DRAWINGS:

Formal drawings annotated in red with proposed changes to address the Examiner's concerns are attached hereto as Appendix C. Proposed changes appear in FIGS. 2, 8, 12, and 13.